ECE 443 / 543 - Computer Architecture
FALL 2013 Syllabus

Instructor: Jonathan Backens
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Lectures: MWF 1100-1150am (Dragas 2106)
Office Hours: MW 300-430pm

Course Description:
An introduction to computer architectures; analysis and design of computer subsystems including central processing units, memories and input/output subsystems; important concepts include datapaths, computer arithmetic, instruction cycles, pipelining, virtual and cache memories, direct memory access and controller design.

Prerequisites:
ECE 341, 346

Pre- or Corequisites:
ECE 304, 489W

Textbook Required:


The Designer’s Guide to VHDL, Third Edition (Systems on Silicon) 2008, By: Peter Ashenden Publisher: Morgan Kaufmann

Software required:
Aldec Active HDL, Altera Quartus II Web Edition

Course Learning Outcomes:
Upon completion of this course, students should
1. Have an extensive knowledge on design of digital computer architecture.
2. Be able to design of arithmetic/logic units, control units, memory subsystems, and input/output units.
3. Be able to design instructions with different addressing modes.
4. Be able to understand register-transfer-level (RTL) design of control and data path, and use software tools such as Aldec Active HDL to simulate hardware designs captured using hardware description language.
5. Be able to analyze the computer performance such as CPU execution time and average memory access time.
6. Be able to understand the fundamental concepts and techniques in computer architecture, including instruction set architecture, pipelining, memory hierarchy and exploitation of instruction-level parallelism.
7. Be able to work in teams to accomplish a project for design and implementation of a RISC (reduced instruction set computer) or VLIW (very long instruction word) pipeline microprocessor and an application system.
8. Be able to write technical reports on high level architecture design and detailed digital system design.

Course Topics:
1. Introduction
2. Classifying computer architecture and instruction sets
3. Review of RISC and Register Transfer Notation
4. CISC vs RISC
5. Central Processing Design
   5.1. Addressing Modes
   5.2. Data paths
   5.3. Control
   5.4. Pipelining
   5.5. Performance
6. Computer Arithmetic
7. Memory Hierarchy
8. Input/Output Systems

Assessment Objectives:
An ability to apply knowledge of mathematics, science, and engineering (Outcome 1)
An ability to design an electrical system, component, or process to meet desired needs, considering all realistic constraints such as economic, environmental, safety, and manufacturability (Outcome 3)
An ability to identify, formulate, and solve electrical and computer engineering problems (Outcome 5)
An ability to use the techniques, skills, and modern engineering tools necessary for computer engineering practice (Outcome 11)
Course Grading:
The grading will be based on two written exams (one midterm, one final), several homework problem sets, lab assignments and a final project. The final grade will be determined by weighing each component as follows:

- Final exam: 30%
- Midterm exam: 30%
- Homework/Labs: 20%
- Final Project: 20%
- Attendance: optional extra 5% (taken randomly during semester)

Make-up Tests and Late Assignments:
Late homework and papers and make-up exams will not normally be permitted. I will give appropriate consideration to documented emergencies, but such arrangements must be made prior to the due date in any situations where the conflict is foreseeable.

Homework:
There will be several assignments during the semester, each weighted equally. You will have one week to work on each of the assignments. While the students are encouraged to discuss the problems amongst each other, each individual should prepare their own answers. All work must be shown for any credit to be awarded. The lowest homework/lab grade will be dropped.

Honor Pledge:
"I pledge to support the honor system of Old Dominion University. I will refrain from any form of academic dishonesty or deception, such as cheating or plagiarism. I am aware that as a member if the academic community, it is my responsibility to turn in all suspected violators of the honor system. I will report to Honor Council hearings if summoned." By attending Old Dominion University you have accepted the responsibility to abide by this code. This is an institutional policy approved by the Board of Visitors. For more information please visit [Honor Council](#)

Special Needs:
Old Dominion University is committed to achieving equal educational opportunity and full participation for persons with disabilities. It is the university's policy that no qualified person be excluded from participation in any university program or activity, be denied the benefits of any university program or activity, or otherwise be subjected to discrimination with regard to any university program or activity. This policy derives from the university's commitment to non-discrimination for all persons in employment, access to facilities, student programs, activities and services. You may view the policy online: Old Dominion University Policies and Procedures 4500 - Accommodation of Students with Disabilities (pdf). For additional information visit the Office of Educational Accessibility online or at 1525 Webb Center.
IMPORTANT DATES

EXAMS

Midterm Exam: October 11 (Friday – during class hour)
Final Exam: TBD

Final Project: Report Due Nov 29th

HOLIDAYS

September 2: Labor Day Holiday (Monday)
October 12-15: Fall Holiday (No Class on Monday)
Nov 27-Dec 1: Thanksgiving Holiday (No Class on Wednesday and Friday)

OTHER DATES

December 6: Last Day of Class (Friday)